Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **B1**
2. **B0**
3. **C1**
4. **COM OUT/IN CN**
5. **IN/OUT C0**
6. **N. E**
7. **VSS**
8. **GND**
9. **S2**
10. **S1**
11. **S0**
12. **A0**
13. **A1**
14. **AN COM OUT/IN**
15. **BN COM OUT/IN**
16. **VCC**

**}CHANNEL IN/OUT**

**}CHANNEL IN/OUT**

**.104”**

**2 1 16 15**

**7 8 9 10**

**3**

**4**

**5**

**6**

**14**

**13**

**12**

**11**

**HC4053**

**DIE ID**

**.118”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: HC4053**

**APPROVED BY: DK DIE SIZE .104” X .118” DATE: 12/15/22**

**MFG: MOTOROLA THICKNESS .010” P/N: 54HC4052**

**DG 10.1.2**

#### Rev B, 7/19/02